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# DESIGNING FOR COST EFFECTIVE FLIP CHIP TECHNOLOGY

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## Designing For Cost Effective Flip Chip Technology

Bump and flip approaches to semiconductor packaging have gained acceptance in the industry. For the designer to take full advantage of this technology, attention to bump composition, bump placement, pitch design, and wafer preparation are required.

### Bump Composition and Placement Guidelines

Metallurgies typically used in wafer bumping are 63-37 SnPb, 90-10 PbSn, 95-5 PbSn, PbIn and a variety of other alloys. Use of the various alloys and compositions depends on the designers application, manufacturing methods, cost sensitivities and other variables. The key elements that the engineer should consider when selecting bump composition and placement include the following:

The wafer bump supplier should be able to maintain alloy control within  $\pm 1\%$ . Typical industry bump heights range from 50. $\mu\text{m}$  to 150. $\mu\text{m}$ . Increasing solder joint height improves fatigue life. Smaller bumps result in less flexibility and less ability of the bump to absorb TCE mismatch and substrate planarity differences. (Mathematical models of this relationship are covered by Coffin-Manson and Engelmaier.) Shorter bumps also necessitate much tighter control of substrate planarity.

Collapse of the bumps in eutectic solders is a function of capture pad diameter on the substrate. Larger capture pads cause the bump to wet out and collapse further. Control of bump collapse is an issue when substrate planarity is considered, and as stated above, taller bumps provide better fatigue life.

As distance to neutral point increases, higher stresses on the corner bumps can cause fatigue failures, therefore corner bumps should be avoided whenever possible. Symmetry of the bump footprint should be avoided, due to optical vision placement requirements of most pick and place machinery. While following the above guidelines, the designer should attempt to place bumps as close to the related silicon circuitry thereby shortening the traces in the die, which reduces associated inductance and other parasitics.

Typical industry guidelines recommend one bump diameter on a given chip/wafer. Different diameters may be achieved with typical bumping processes, but the different bump heights, collapsibility, and contact problems would adversely impact manufacturability and reliability.

Not all pads on the die have to have a bump. Select pads can be masked off and used for probe or other test or placement requirements.

## **Pitch Selection Insures Manufacturability and Cost Effectiveness**

The most critical aspect of the bump and flip process is the bump pitch, which when designed correctly, provides reduced cost and improved reliability. These general concepts need to be understood during the design phase when attempting to move into flip chip attach.

In general, the flip chip attach bump pitch should be as wide as possible. Most wafer bumping processes allow pitches of 200 $\mu$ m or less. This may be necessary for certain applications, ultra-high I/O ASIC's for example. But as I/O increases, it is recommended that the designer redistribute the I/O on the die to accommodate wider pitches in the range of 250 to 500 $\mu$ m. Wider pitches offer the designer these significant advantages:

Routing in the substrate, BGA or CSP package, PWB, etc., can be simplified. Substrates represent the highest portion of the packaging cost. Wider pitches provide relief to substrate technology escape routing and enable simpler and less costly substrates.

Wider pitches reduce the potential of bump to bump shorting during the reflow processing, provide space under the die for cleaning, and enable effective underfilling. In addition expanded bump pitch allows the wafer bumper to widen the UBM (under bump metal) structures. This leads to taller bumps. Taller bumps or standoff provide improved fatigue life, cleaning under the die, underfill flow, and improved tolerance of board flatness variations. And finally wider pitch facilitate larger diameter bumps which provide better current carrying capability and reduced electromigration.

While maintaining the widest pitch possible, it is preferred to maximize the bump count on any die. Fatigue life can be improved by maximizing bump count due to the constraint provided by each bump in a given area. With decreased bump count, the substrate and chip still expand at their different TCE's which creates greater stress on fewer bump positions. The use of underfills, which absorb TCE mismatch, will minimize this concern.

Many flip chip designs today implement various pitches onto a given die/wafer to accommodate optical vision requirements, thermal dissipation needs, underfill requirements, electrical routing, etc.

## **Metallurgical Considerations**

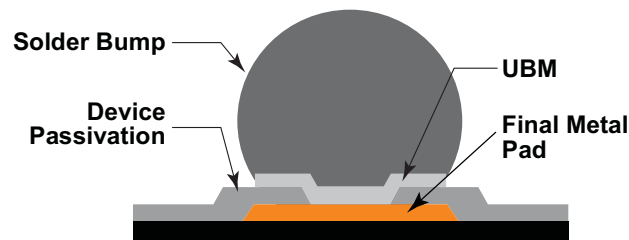
Industry wafer bumping techniques today require the implementation of an under bump metal (UBM) or bump limiting metal on top of the die pad. (Shown in figure 1.) The user should insure that the under bump metal structures employed by the wafer bumping facility be constructed with consideration of the film stresses

associated with the material. Film stresses exerted on the die pads during reflow can create silicon cratering and other reliability problems. Sputtered Aluminum - Nickel - Copper, evaporated Chrome-Copper and electroless nickel are typical industry UBM films that exhibit low film stress.

Features of low stress films include TCE and ductility match to the die pads. Precise thickness control of the UBM structures contributes to low stress characteristics as well. Not all UBM structures and bump techniques allow wafer probing prior to bumping. The Al-Ni-Cu UBM structure accommodates this.

The selection of high lead, eutectic Sn-Pb, or other bump alloy is dependent on application, cost sensitivity, and process environment. Eutectic solders allow the same processing and temperature profiles as SMT devices, at 215° to 230°C. Lower cost laminates can typically be used with eutectic whereas high lead bumps require high performance substrates, ceramics, or additional solder screening at the board level. Use of eutectic bumps can preclude the need for a solder mask on the laminate board as well as screen printing pastes needed to connect with high lead bumps. Finally, eutectic bumps are harder than high lead bumps and can be probed with more pressure insuring better contact

**Figure 1 –**  
Cross Section of Typical  
Bump Structure



Alpha particle considerations are related to traces of isotopes Pb210, Pb214, Thorium, and Polonium contained in lead as it decays. Chip sensitivity to these emissions increases as channel width geometries and critical node dimensions get smaller, creating potential bit errors. The silicon designer should determine how close a bump can be placed near an alpha sensitive node or circuit. In particular, DRAM circuits, SRAM based circuits, Flash memories and sensitive logic should be evaluated for potential alpha particle sensitivity.

The use of high lead bumps can exacerbate this issue. Use of low alpha solders or non-lead solders reduces the problems.

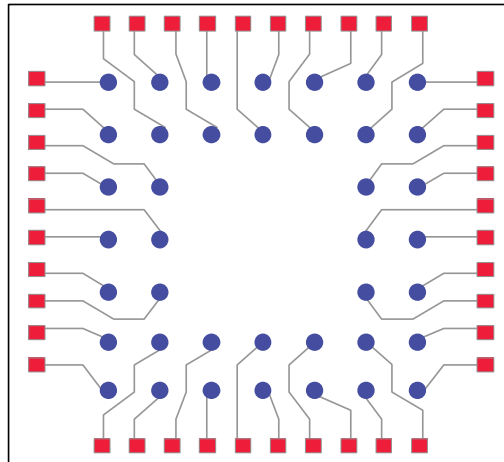
## Die Surface Area Utilization and Redistribution

One of the major advantages of flip chip technology is that it allows the chip designer to place I/O, power, etc. on virtually any position on the surface of the die. Unencumbered by perimeter pad limitations, the designer can increase die pad count, shrink die while maintaining pad count and eliminate pad limited silicon.

The industry is moving today toward chip designs with area array or multiple row pads on the die. Concurrently, redistribution is a wafer level enabling technology that will allow more users to gain the advantages of bump and flip packaging. The user can implement flip chip technology on existing perimeter wire bond die where the pitch is too close to allow standard bump pitches. This technique reroutes the I/O, signals, clock and power pads to dual or multiple rows or full array on the die surface. Any perimeter arrangement of pads can be redistributed for flip chip attach as the redistribution traces are typically 35µm. (See figure 2.)

With this technology the die footprint can be designed to match CSP standards being developed by JEDEC. Perhaps more importantly, pad pitch can be expanded allowing larger bumps, more effective escape routing on the substrate and the other advantages described above.

**Figure 2 –**  
Example of Redistribution  
from a Perimeter to Array  
Pad Locations



Key issues the designer must address when preparing an IC for redistribution include: 1) Care where bumps are placed relative to possible alpha particle effects on sensitive areas of the die. Low alpha solders and non lead solders are available to address this issue. 2) Attention to the added inductance associated with redistribution in high frequency applications. 3) Proper passivation to prevent pin hole problems in the redistribution process. 4) Depopulation or bump position to optimize underfill processing in the flip chip attach step.

Properly applied, bumps can be placed in virtually any position on a die, given the pitch considerations mentioned above. The designer can optimize I/O count for increased power, ground and clock performance through the use of redundant bumps. “Dummy bumps” can be added for symmetry, additional thermal management, or to optimize interconnect to reduce inductance and enhance speed. Dummy bumps can also be used for mechanical stability. Fatigue life can be improved by maximizing bump count because of the constraint provided by each bump. With fewer bumps, the substrate and chip can expand at their different

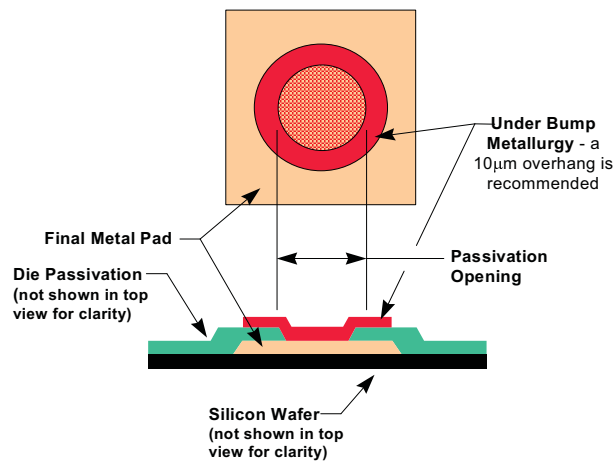
TCE's and present higher stress on less bumps. Other reasons for dummy bumps are chip orientation and optical alignment during placement.

Designing bump layout for future die shrinks is an advantage of redistribution and flip chip attach. From the chip design perspective, consideration can be given to anticipated shrinks and create flip chip arrays on the die that accommodate future shrinks with the same flip chip footprint, possibly eliminating the need for substrate redesign. If dummy bumps are involved, the designer should place these, and any extra power or ground bumps and other non critical bumps on the outside rows of an array, leaving the interior for necessary bumps. After the shrink the same footprint of necessary bumps can remain the same.

## Wafer, Passivation, and Die Considerations

Any of the common wafer diameters (100mm, 125mm, 150mm and 200mm) are acceptable for most industry bumping processes. The designer wanting to utilize bump and flip technology should be aware of the requirements related to final metal pad dimensions, shape and passivation opening dimensions. Depending on the bump attach process and UBM metallurgy most passivation types are acceptable. Oxi nitride, silicon oxide, silicon nitride, polyimide, and BCB are all appropriate in most cases.

**Figure 3 –**  
Ideal Passivation Opening  
Design for Bumping.



Double layer passivation is preferred, particularly if redistribution is involved, as this prevents possible pin holes and provides better planarity to the wafer surface for the redistribution traces, with 8KÅ to 12KÅ thickness.

The passivation openings are also an important to the silicon designer preparing a die for bump and flip. Wider openings allow better bonding of the UBM to a larger area This in turn provides better shear strength, fatigue life, reliability, and current carrying capacity. Openings of ~80.µm are required to achieve a typical 115.µm to 130.µm high bump which will improve these characteristics. (See Figure 3.)

Wafer diameter, die size and subsequent total die/good die per wafer, and wafer bumping cost determine cost per die to bump.

## **Packaging and Shipping Issues**

For tape and reel packaging, where the die is to be packaged bumps down, allow .010" to .020" ledge around the die for it to ride on the ledge of the tape pocket. This distance can vary depending on the type of tape used. Other approaches include a pedestal for the die to sit on in non full array applications.

Gel Pack, waffle pack or similar packaging options may provide a suitable alternative to tape and reel. A single size may accommodate various die sizes, precluding the need for different pocket sizes of T&R. Other costs associated with this approach need to be evaluated on a case by case basis.

## **Flip Chip Attach Processing and Substrate Issues**

Flip chip attach processing must include analysis of substrate selection, pick and place equipment, reflow processing, cleaning, underfill selection and dispense, and economic considerations. These issues are beyond the scope of this paper and are addressed in other work.

## **Electron Physics and Thermal Considerations**

- Electromigration is a function of current density and cross section of the bump and final metal pad opening diameter. If the designer can double the cross sectional area, the result is 4X the current carrying capacity. Larger passivation openings allow larger UBM structure, and hence larger diameter bumps and generally provide better current carrying capacity, improved shear strength and fatigue life.
- Continuous current carrying capability for bumps based on a 102 $\mu$ m passivation opening, at 150°C max junction temp, is 340mA.
- Bump resistance and inductance are lower than those of packaged device leads or CSP interconnect leads. Combined bump and UBM inductance is typically in the  $\leq 0.2$ nH range and resistance is measured below 30m $\Omega$ . The testing and measurement of these values necessarily includes the trace connections between adjacent test bumps and will result in values that are not indicative of the values of the bumps alone.

- Thermal resistance of a bump can be calculated as follows:

$$\theta = \frac{h}{Ak}$$

$\theta$  = thermal resistance of the material, °C/W

$h$  = bump height or material thickness,  $\mu\text{m}$

$A$  = cross-sectional area of the material,  $\mu\text{m}^2$

$k$  = thermal conductivity of the material, W/mK

Thermal conductivity of eutectic 63-37 solder is approximately 0.50 W/cm °K. Given a solder bump that is 120.µm high and approximately cylindrical, with a cross sectional area of  $1.27 \times 10^4$ , the thermal resistance would be 186 OC/W. Including the thermal resistance of the UBM structure increases total thermal resistance by less than 0.5%.

Beyond the thermal conductivity of the bumps, factors impacting heat dissipation include underfill selection, standoff/bump height, architectural efficiency and pad placement on the silicon, and substrate type.



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